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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/718,892	JAWARANI ET AL.
	Examiner	**Art Unit**
	Heather A. Doty	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 28 July 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3,7-14,17-28,30,31,34-36 and 42-46 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,7-14,17-28,30,31,34-36 and 42-46 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 1, 26, 34, 36, 44, and 45 are objected to because of the following informalities: In all cases, "atoms per centimeter squared" should be inserted after "at a dose not exceeding 1E17." Appropriate correction is required.

Claims 1-3 are objected to because of the following informalities: In all cases, "atoms" should be replaced with "germanium." Appropriate correction is required.

Claims 14 and 22-25 are objected to because of the following informalities: In all cases, "particles" should be replaced with "germanium." Appropriate correction is required.

Claim 26 is objected to because of the following informalities: In line 3, "of the" should be removed and "particles" should be replaced with "germanium," so that the line reads "the implanting further includes implanting the germanium..." In line 6, "of the particles" should be removed so that the line reads "germanium implanted into the..." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 36 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Lines 7-10 of claim 36 recite "implanting a source/drain dopant into the source/drain region, wherein the implanting the source/drain dopant is performed subsequent to the increasing the lattice constant at a dose not exceeding 1E17." It is not clear whether the limitation "at a dose not exceeding 1E17" refers to the implanting the source/drain dopant or to the increasing the lattice constant. Since the specification is silent regarding the preferred dose used for the source/drain dopant implant, the examiner assumes that "at a dose not exceeding 1E17" refers to the increasing the lattice constant (by implanting germanium), as disclosed in the instant specification in line 5 of page 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 7, 9, 19, 21-24, 26, 27, 34, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), considered with Murakushi (U.S. 5,770,512) for a showing of inherency for claims 3, 36, and 45.

Regarding claim 1, Aronowitz et al. teaches method of forming a contact to a source/drain contact region of a transistor device having a gate (**38** in Fig. 2B) and the source/drain contact region (**34/36** in Fig. 2B) is comprised substantially of silicon (**14** in

Fig. 2B), the method comprising: implanting germanium into a region of the source/drain contact region at a dose not exceeding 1E17/cm^2 (column 2, lines 35-36, column 3, lines 41-44; Fig. 2A); activating the germanium implanted into the source/drain contact region (column 3, lines 46-48; column 2, lines 37-41; instant specification, p. 4, lines 6-9); implanting a source/drain dopant into the source/drain contact, wherein the implanting the source/drain dopant is performed subsequent to the activating the germanium (column 3, lines 60-64); and forming a metal silicide over the source/drain contact region after the activating to form the contact (column 4, lines 52-68). Aronowitz does not teach that the metal silicide is a nickel silicide.

Kluth et al. teaches a method of forming source/drain contacts including forming a metal silicide wherein the metal silicide is characterized as nickel silicide (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Aronowitz et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20).

Regarding claim 2, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that activating the atoms further includes activating the atoms in order to make the atoms substitutional in a lattice of the source/drain region, wherein the lattice includes atoms of the first material (column 1, lines 64-66).

Regarding claim 3, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that activating the atoms increases a lattice constant of the lattice in the source/drain contact region (Si has lattice constant 0.543 nm, Ge has lattice constant 0.566 nm, SiGe has lattice constant between 0.543 and 0.566 nm, depending upon the Ge concentration, see U.S. 5,770,512 to Murakoshi et al.).

Regarding claims 7 and 9, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that the activating includes heating the source/drain contact region to a temperature of 900°C (column 2, lines 39-40).

Regarding claim 19, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that the gate is over a semiconductor substrate, the source/drain contact region is in the semiconductor substrate, and the source/drain contact region is disposed laterally from the gate (Fig. 2B).

Regarding claims 21-24, Aronowitz et al. and Kluth et al. together teach the method of claim 19 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that the implanting the particles further includes implanting with an energy of 40 keV and a dose of 2E16 atoms per centimeter squared (column 2, lines 35-36).

Regarding claim 26, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that the transistor has a second source/drain contact; the implanting further includes

implanting the particles into the second source/drain contact region at a dose not exceeding 1E17/cm^2 (column 2, lines 35-36, column 3, lines 41-44); the activating of the germanium further includes activating the germanium implanted into the second source/drain contact region; and the implanting of the source/drain dopant further includes implanting the source/drain dopant into the second source/drain contact region; further comprising forming a second metal silicide over the second region to form a second contact (Fig. 2A-2B; column 4, lines 63-67).

Regarding claim 27, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches that the source/drain dopant includes boron (column 3, lines 60-64).

Regarding claim 34, Aronowitz et al. teaches a method of forming a semiconductor device, the method comprising implanting germanium into a region of a silicon substrate (**14** in Fig. 2B) at a dose not exceeding 1E17/cm^2 (column 2, lines 35-36, column 3, lines 41-44); activating the germanium implanted into the region of the substrate with a non-diffusion activation process (oxidation anneal is performed for as short a time as possible to prevent germanium diffusion, see column 2, lines 52-55); and forming a metal silicide over the region after activating (column 4, lines 52-68). Aronowitz does not teach that the metal silicide is a nickel silicide.

Kluth et al. teaches a method of forming source/drain contacts including forming a metal silicide wherein the metal silicide is characterized as nickel silicide (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Aronowitz et al. and forming a nickel silicide, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20).

Regarding claim 45, Aronowitz et al. teaches in a transistor device structure having a gate stack (**38** and oxide in Fig. 2B) and source/drain contact regions comprised primarily of a first material (silicon, **14** in Fig. 2B), wherein the source/drain contact regions have a lattice constant, a method of forming a contact, comprising implanting germanium at a dose not exceeding 1E17/cm^2 (column 2, lines 35-36, column 3, lines 41-44) into the source/drain contact regions (column 1, lines 64-66; column 3, lines 41-44; Fig. 2A); activating the germanium implanted into the source/drain contact regions to increase the lattice constant of the source/drain contact regions (column 3, lines 46-48); forming a metal silicide over the source/drain contact regions after the activating of the atoms (column 4, lines 52-68). Aronowitz et al. does not teach that the metal silicide is a nickel silicide.

Kluth et al. teaches a method of forming source/drain contacts including forming a metal silicide wherein the metal silicide is characterized as nickel silicide (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by Aronowitz et al. and forming a nickel silicide, as taught by Kluth et al. The motivation

for doing so at the time of the invention would have been to produce a silicide that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20).

Regarding claim 46, Aronowitz et al. and Kluth et al. together teach the method of claim 45 (note 35 U.S.C. 103(a) rejection above). Aronowitz et al. further teaches doping the source/drain contact regions with p-type material after activating the atoms and prior to forming the metal silicide (boron, column 3, lines 60-64).

Claims 36, 42, 43, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over An et al. (U.S. 6,706,614) in view of Kluth et al. (U.S. 6,486,062).

Regarding claims 36 and 42, An et al. teaches a method of forming a semiconductor device, the method comprising forming a gate (**34** in Fig. 5b) over a silicon substrate (**18** in Fig. 5; column 4, lines 36-43), the substrate having a lattice having a lattice constant; increasing the lattice constant of the lattice in a source/drain region of the substrate after the forming the gate by implanting germanium (column 5, lines 12-22); and implanting a source/drain dopant into the source/drain region (boron—further limited by claim 42--column 4, line 65 – column 5, line 1), wherein the implanting the source/drain dopant is performed subsequent to the increasing the lattice constant (column 5, lines 28-30) at a dose not exceeding 1E17/cm^2 (column 5, lines 12-22).

An et al. does not teach forming a nickel silicide over the portion of the source/drain region.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by An et al. and further forming a nickel silicide over the portion of the source/drain region, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a contact that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20).

Regarding claim 43, An et al. and Kluth et al. together teach the method of claim 36 (note 35 U.S.C. 103(a) rejection above). An et al. further teaches that the source/drain dopant includes a source/drain extension dopant for forming a source/drain extension in the substrate (column 4, lines 44-53).

Regarding claim 44, An et al. teaches a method of forming a semiconductor device, the method comprising: forming a gate (**34** in Fig. 5b) over a silicon semiconductor substrate (**18** in Fig. 5; column 4, lines 36-43); implanting particles including germanium into a region of the substrate after forming the gate (Fig. 2A) at a dose not exceeding 1E17/cm^2 (column 5, lines 12-22); activating the germanium implanted into the region (column 5, lines 23-28); and implanting a source/drain dopant into the source/drain region (column 4, line 65 – column 5, line 1), wherein the implanting the source/drain dopant is performed subsequent to the activating the germanium (column 5, lines 28-30).

An et al. does not teach forming a nickel silicide over the portion of the source/drain region.

Kluth et al. teaches a method of forming source/drain contacts including forming a nickel silicide (column 4, lines 36-38).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method taught by An et al. and further forming a nickel silicide over the portion of the source/drain region, as taught by Kluth et al. The motivation for doing so at the time of the invention would have been to produce a contact that forms a first low-resistivity phase at relatively low temperatures (column 2, lines 15-20).

Claims 8, 14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), as applied to claims 1 and 19 above, and further in view of Erokhin et al. (U.S. 2003/0087504).

Regarding claims 8, 14, and 25, Aronowitz et al. and Kluth et al. together teach the method of claims 1 and 19 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating includes heating the source/drain contact region to a temperature greater than 1000 °C—as further limited by claim 8—or implanting the particles is performed at a temperature between 25 and 600 °C—as further limited by claims 14 and 25.

Erokhin et al. teaches a method of implanting germanium into silicon at a temperature between 25 and 600 °C (paragraphs 0011-0012) and subsequently annealing at a temperature greater than 1000 °C (paragraph 0048).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Aronowitz et al. and Kluth et al.

together and Erokhin et al. by forming contact to a source/drain region of a transistor using the method of claim 1, as taught by Aronowitz et al. and Kluth et al. together, by implanting germanium at a temperature between 25 and 600 °C and annealing the germanium implant at a temperature of 1100°C, as taught by Erokhin et al., since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art (*In re Aller*, 105 USPQ 233 (CCPA 1955)).

Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 1 above, and further in view of Downey (U.S. 2002/0187614).

Regarding claims 10-11, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating further includes rapid thermal annealing or laser annealing of the source/drain contact regions.

Downey teaches a method of implanting silicon with germanium and activating the germanium by rapid thermal annealing and laser annealing (paragraph 0032).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Aronowitz et al. and Kluth et al. together and Downey by forming a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Aronowitz et al. and Kluth et al. together, by activating the germanium implant by rapid thermal annealing or laser annealing, as taught by Downey. The motivation for doing so at the time of the invention

would have been to cause chemical bonding between the substrate and the implanted material, as taught by Downey (paragraph 0031).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 1 above, in view of Imai (U.S. 5,506,427).

Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating further includes arc lamp thermal annealing of the source/drain contact region.

Imai teaches a method of annealing SiGe by arc lamp annealing (column 6, lines 7-10).

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Aronowitz et al. and Kluth et al. together and Imai by forming a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Aronowitz et al. and Kluth et al. together, by activating the germanium implant by laser arc annealing, as taught by Imai. The motivation for doing so at the time of the invention would have been to avoid degrading transistor characteristics, as expressly taught by Imai (column 5, line 66 – column 6, line 2).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 1 above, and further in view of Murakoshi et al. (U.S. 5,770,512).

Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach that the activating includes gas convection annealing of the source/drain contact region.

Murakoshi et al. teaches a method of activating germanium ion-implanted into silicon by convectively heating it in a nitrogen gas atmosphere at 550°C for an hour to recrystallize the silicon wafer following ion implantation (column 14, lines 44-52).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region according to the method of claim 1 as taught by Aronowitz et al. and Kluth et al. together, and use gas convection annealing to activate the germanium implantation, as taught by Murakoshi et al. The motivation for doing so at the time of the invention would have been to recrystallize the silicon wafer following ion implantation, as noted above and taught by Murakoshi et al.

Claims 17, 18, 20, 28, 30, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), as applied to claims 1 and 19 above, and further in view of Chakravarthi et al. (U.S. 6,797,593).

Regarding claims 17 and 18, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach forming a sidewall spacer adjacent to a sidewall of the gate, wherein the implanting the germanium is performed prior to the forming the sidewall spacer and wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant.

Chakravarthi et al. teaches a method for forming a MOSFET drain extension activation, including forming a sidewall spacer adjacent to the sidewall of the gate and implanting arsenic into drain extension regions, wherein the implanting the arsenic (**314** in Fig. 4A) is performed prior to the forming the sidewall spacer (**318** in Fig. 4A; column 2, lines 25-38) and wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant (**320** in Fig. 4A).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region of a transistor device using the method of claim 1, as taught by Aronowitz et al. and Kluth et al. together, and further form a sidewall spacer adjacent to a sidewall of the gate, wherein the implanting the germanium is performed prior to the forming the sidewall spacer, and wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant, as taught by Chakravarthi et al. The motivation for doing so at the time of the invention would have been to use the sidewall spacers to mask the implantation of the source/drain dopant, as taught by Chakravarthi et al. (column 3, line 65 – column 4, line 3), after the particle implantation.

Regarding claim 20, Aronowitz et al. and Kluth et al. together teach the method of claim 19 (note 35 U.S.C. 103(a) rejection above) but do not teach implanting a second source/drain dopant in the semiconductor substrate after the implanting the source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant.

Chakravarthi et al. teaches implanting a second source/drain dopant (**320** in Fig. 4A;) in the semiconductor substrate after the implanting the source/drain dopant (drain extensions, **314** in Fig. 4A), wherein the second source/drain dopant is implanted deeper than the source/drain dopant (see Fig. 3, which shows that the extension implants are less deep than the subsequent source/drain dopant implants).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region by using the methods of claims 1 and 19, as taught by Aronowitz et al. and Kluth et al. together, and further implant a second source/drain dopant in the semiconductor substrate after the implanting the source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant, as taught by Chakravarthi et al. The motivation for doing so at the time of the invention would have been to form drain extensions and thereby combat channel hot carrier effects, as taught by Chakravarthi et al. (column 2, line 11).

Regarding claim 28, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), wherein the gate is over a semiconductor substrate and a channel is in the substrate under the gate, but does not teach forming a source/drain extension adjacent to the channel in the semiconductor substrate.

Chakravarthi et al. teaches forming a source/drain extension adjacent to the channel in the semiconductor substrate (column 2, lines 25-26) to combat channel hot carrier effects (column 2, line 11).

Therefore, at the time of the invention, it would have been obvious to form a contact to a drain/source contact region using the method according to claim 1 and as taught by Aronowitz et al. and Kluth et al. together, and further form a source/drain extension adjacent to the channel in the semiconductor substrate, as taught by Chakravarthi et al., to combat channel hot carrier effects, as noted above as expressly taught by Chakravarthi et al.

Regarding claim 30, Aronowitz et al. and Kluth et al. and Chakravarthi et al. together teach the method of claim 28 (note 35 U.S.C. 103(a) rejection above). Chakravarthi et al. further teaches implanting a second source/drain dopant into the substrate for forming the source/drain extension (**314** in Fig. 4A), wherein the implanting the second source/drain dopant is performed prior to the implanting the source/drain dopant (**320** in Fig. 4A).

Regarding claim 31, Aronowitz et al. and Kluth et al. together teach the method of claim 1 (note 35 U.S.C. 103(a) rejection above), but do not teach further activating the source/drain dopant.

Chakravarthi et al. teaches activating the source/drain dopant (**322** in Fig. 4A) to diffuse implanted dopants to a final drain extension junction depth (column 12, lines 6).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a contact to a source/drain contact region according to the method of claim 1, as taught by Aronowitz et al. and Kluth et al. together, and further activate the source/drain dopant, as taught by Chakravarthi et al., to cause the dopants to diffuse to a desired drain extension junction depth.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aronowitz et al. (U.S. 5,296,387) in view of Kluth et al. (U.S. 6,486,062), as applied to claim 34 above, and further in view of Gibbons (U.S. 4,243,433).

Aronowitz et al. and Kluth et al. together teach the method of claim 34 (note 35 U.S.C. 103(a) rejection above), but do not teach that the non-diffusion activation process includes one of arc lamp rapid thermal annealing of the region and laser annealing of the region.

Gibbons teaches a method of activating an ion implantation non-diffusively using laser annealing (column 4, lines 4-25).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a semiconductor device according to the method of claim 34, as taught by Aronowitz et al. and Kluth et al. together, wherein the non-diffusion activation process includes laser annealing of the region, as taught by Gibbons. The motivation for doing so at the time of the invention would have been to avoid lateral spread of the dopants and thereby reduce device size, as expressly taught by Gibbons (column 1, lines 13-19).

Response to Arguments

Applicant's arguments filed 28 July 2005 have been fully considered but they are not persuasive.

As amended, independent claims 1, 34, 36, 44, and 45 now include the limitation that germanium be implanted into source/drain regions of a silicon substrate at a dose not exceeding $1E17/cm^2$. Applicant argues that although Aronowitz et al. actually

implants at $2E16/cm^2$, he forms a layer of oxide that increases the germanium concentration (see Arguments, pg. 8, fourth paragraph). However, as currently written, claims 1, 34, 36, 44, and 45 limit the implant dose only, and not the final concentration of germanium in the source/drain regions of the silicon substrate. Therefore, Aronowitz et al. does disclose the limitation of implanting germanium into the source/drain regions at a dose not exceeding $1E17/cm^2$.

Applicant also argues that Aronowitz does not teach implanting germanium into the source/drain regions after forming the gate (see Arguments, pg. 8, fourth paragraph), and that independent claims 1, 36, 44, and 45 all require that the gate be present before the germanium implant. However, claims 1 and 45 do not include language that requires the gate to be present prior to the germanium implant. In claims 1 and 45, the presence of the gate is disclosed only in the preambles, and no method step specifies when the gate is formed. Regarding claims 36, 44, and their dependent claims, the argument is moot in view of the new grounds of rejection.

Finally, as amended, all of the independent claims specify that the metal silicide is nickel silicide. Applicant argues that the possible benefits of nickel silicide do not appear to have been known at the time of Aronowitz et al., and that there is no suggestion of a solution to the spiking problem of nickel silicide in Kluth et al. (pg. 9, first full paragraph). However, this argument is not persuasive because the benefits of nickel silicide *were* known at the time of the instant invention, and it is not necessary for Kluth et al. to address the problem of spiking in nickel silicide, since Kluth et al. does teach a benefit of using nickel silicide in source/drain contacts.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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